

2023
DESIGN AND VERIFICATION™
DVCON
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EUROPE
10 YEAR ANNIVERSARY

DVCON EUROPE
2023
CONFERENCE
PROGRAM

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DVCon Europe 2023



Welcome Message from DVCon Europe General Chair,
Martin Barnasconi
General Chair - NXP Semiconductors

Dear friends of DVCon Europe,

I am really happy to welcome you again to the Design and Verification Conference & Exhibition in Europe (DVCon Europe), and especially this year as we celebrate our 10th anniversary edition! This year's conference will be held on the 14th and 15th of November in the Holiday Inn Munich City Center. DVCon Europe is the premier European technical conference on system, software, design, verification, validation, and integration. It is a place to share and discuss the latest methodologies and technologies for the industrial use of standards, languages and tools.

In 2013 we started the preparation of the first DVCon Europe, held in October 2014 in Munich, Germany. At that time, there was only one DVCon, a well-established and recognized conference in Silicon Valley. "Could we bring this success story to Europe?" was one of my first questions to a small team of industry experts in Europe. I quickly noticed that we all had the same ambition: to establish a new venue where Design and Verification engineers and companies active in Electronic Design Automation can network, interact and exchange industry best practices and experiences. DVCon Europe was born!

Now, 10 years later, it is great to see that DVCon Europe is an established conference and continues to attract more companies and engineers. And after launching DVCon Europe, we've seen expansion of DVCon conferences to other regions in the world, such as India, China, Taiwan and Japan. DVCon has become an event with global coverage!

For those who joined us for the first edition of DVCon Europe back in 2014, you might remember the co-located FDL conference, focusing on academic contributions and research on specification and design languages. Also back then, we had the ambition to connect research with industry, but in the years that followed the DVCon Europe program primarily focused on the industrial application of design technologies and methodologies.

Therefore I am happy to announce that for DVCon Europe 2023 we are strengthening the connection to the academic and research institutes by introducing a "Research track", which is fully embedded into the technical program. We invited renowned professors to help us with this, and they established a new committee with experts from various universities to conduct the scientific review of the papers submitted to this new research track.

The technical program in DVCon Europe remains untouched: It includes compelling keynotes, in-depth tutorials, energetic panels, and industry-relevant paper presentations focusing on sharing best practices when using the latest technologies, languages and tools. Furthermore, DVCon Europe hosts an Expo showcasing EDA and IP solutions and services, and we encourage all participants to interact with these exhibitors, and enjoy the networking with your industry peers!

DVCon Europe is also actively driving the standards and since 2016 we added the SystemC Evolution Day as a technical forum to discuss current and future standardization topics for inclusion in Accellera and IEEE standards. Also this year the SystemC community will meet on the 16th of November to advance the SystemC standard.

I look forward to meet you again in Munich, to celebrate a successful 10 years of DVCon Europe, and to encourage the collaboration between industry and academic to further grow the conference in the years to come!

Martin Barnasconi
DVCon Europe General Chair 2023

CONFERENCE SPONSOR



SYSTEMS INITIATIVE

Accellera Systems Initiative is an independent, not-for profit organization dedicated to create, support, promote, and advance system-level design, modeling, and verification standards for use by the worldwide electronics industry. We are composed of a broad range of members that fully support the work of our technical committee to develop technology standards that are balanced, open, and benefit the worldwide electronics industry. Leading companies and semiconductor manufacturers around the world are using our electronic design automation (EDA) and intellectual property (IP) standards in a wide range of projects in numerous application areas to develop consumer, mobile, wireless, automotive, and other "smart" electronic devices. Through an ongoing

partnership with the IEEE, standards and technical implementations developed by Accellera Systems Initiative are contributed to the IEEE for formal standardization and ongoing governance.

Our Mission

At Accellera our mission is to provide a platform in which the electronics industry can collaborate to innovate and deliver global standards that improve design and verification productivity for electronics products.

The purposes of the organization include:

- » Provide design and verification standards required by systems, semiconductor, IP, and design tool companies to enhance a front-end design automation process.
- » Collaborate with our community of companies, individuals, and organizations to deliver standards that lower the cost of designing commercial IC and EDA products and embedded system solutions, as well as increase the productivity of designers worldwide.
- » Encourage availability and adoption of next-generation EDA and IP standards that encompass system-level, RT-level, and gate-level design flows.
- » Collaborate with the electronic design community to deliver standards that increase designer productivity and lower the cost of product development.
- » Provide mechanisms that enable the continued growth of the Accellera Systems Initiative user community including SystemC, Universal Verification Methodology (UVM), and IP-XACT.
- » Standardize technical implementations developed by Accellera Systems Initiative through the IEEE.

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Technical Program Grid – Day 1 – Tutorials – November 14

	Forum 4	Forum 5	Forum 6	Forum 7	Großer Saal
8:30 – 8:45 AM	Opening Session (Ballsaal)				
8:45 – 9:45 AM	Keynote: Philippe Notton Energy-efficient High Performance Compute, at the heart of Europe (Ballsaal)				
9:45 – 10:00 AM	Attendee Break (Großer Saal)				Exhibit Hall Open
10:00 – 11:30 AM	T1.1 Introduction into IP-XACT	T2.1 Accellera Functional Safety Working Group Update and Next Steps	T3.1 Scalable agile processor verification using SystemC UVM friends	T4.1 SysML v2: An overview with demonstration	
11:30 – 11:45 AM	Attendee Break (Großer Saal)				
11:45 – 1:15 PM	T1.2 AI-Driven Debug and Verification Management 	T2.2 Shift your HDL design left and keep your eyes on team code metrics in FPGA & ASIC design and verification 	T3.2 Model-Based Approach for Developing Optimal HW/SW Architectures for AI systems 	T4.2 New Methods in Core and SoC Verification based on RISC-V 	
1:15 – 2:15 PM	Lunch (Großer Saal)				
2:15 – 3:45 PM	T1.3 IP-XACT Industrial Practices	T2.3 Migrating from UVM to UVM-MS	T3.3 Making the impossible possible: CDC and RDC closure with abstracts from different tools	T4.3 Open-Source Virtual Platforms for Industry and Research	
3:45 – 4:00 PM	Attendee Break (Großer Saal)				
4:00 – 5:30 PM	T1.4 How to leverage the power of MATLAB from Functional Verification Test Benches 	T2.4 The Expanding role of Static Signoff in Verification Coverage 	T3.4 Exploring New Frontiers of High-Performance Verification with UVM-AMS 	T4.4 Double Software Verification Shift-left by combining Model-Based Design and Virtual ECUs'  	
5:30 – 7:00 PM	Reception (Großer Saal)				
7:30 – 10:30 PM	Anniversary Dinner (Hofbräukeller)		sponsored by: 		

Technical Program Grid - Day 2 - November 15

	Forum 4	Forum 5	Forum 6	Forum 7	Forum 8	Großer Saal
8:00 – 8:15 AM	Opening Session (Ballsaal)					
8:15 – 9:15 AM	Keynote Speaker: Michaela Blott Pervasive and Sustainable AI with Adaptive Computing (Ballsaal)					
9:15 – 10:15 AM	Panel: “All AI All the Time” Poses New Challenges for Traditional Verification (Ballsaal)					
10:15 – 10:30 AM	Attendee Break (Großer Saal)					Exhibit Hall Open
10:30 – 12:00 PM	P1.1 A Hybrid Approach For Interrupts Verification Verification of an AXI cache controller using multi-thread approach based on OOP design patterns [Short] Hybrid Emulation for faster Android Home screen bring up and Software Development [Short] A perfect blend of verification techniques, platforms, and AI-empowered debugging in Ethernet Subsystem Verification	P2.1 SV VQC UDN for Modeling Switch-Capacitor-based Circuits Self-Triggering Mechanism for Modeling a Low-Dropout Regulator with Load Capacitor **[Short] On the Performance Differences of SystemC and SystemC AMS: A Guideline for Real Number Modeling and Beyond **[Short] A tool for Investigating Cyber-Physical Systems via SystemC AMS Virtual Prototypes Derived from SysML Models	P3.1 [Short] A Model-Based Reusable Framework to Parallelize Hardware and Software Development Fuzzing Firmware running on Intel® Simics® Virtual Platforms [Short] 400G IPU Case Study: Demonstrating Shift-left of Soft Logic RTL Development on Real World Design using Intel Agilex FPGA SystemC Model **Co-Design of Automotive Boardnet Topology and Architecture	P4.1 Verilator + UVM-SystemC: a match made in heaven Closed-Loop Model-First SoC Development With the Intel Simics Simulator ** [Short] A Compositional Simulation Framework for Testing Adversarial Robustness of Deep Neural Networks ** [Short] Large-scale Gatelevel Optimization Leveraging Property Checking	P5.1 [Short] An Improved Methodology for Debugging UPF Issues at SoC level Power Aware Simulations Unified Architecture of L1 and L2 Cache with Low Power Extensions for Multi-Core UVM-based Library Package Virtual testing of overtemperature protection algorithms in automotive smart fuses [Short] Efficient Verification of a RADAR SoC Using Formal and Simulation-Based Methods	
12:00 – 1:00 PM	Lunch (Großer Saal)					
1:00 – 2:30 PM	P1.1 A scalable VIP component to increase robustness of co-verification within an ASIC A Novel Framework to Accelerate System Validation on Emulation [Short] Low-Power Validation Framework for Standard Cell Library including Front-End and Back-End implementation [Short] Initialization Techniques for D-Flip-Flop Based Scan Chain with Scan Flush Architecture in Gate-Level Simulation	P2.2 System-Level Simulation of a SPAD-Based Time-of-Flight Sensor in SystemVerilog **Clock Tree Design Considerations in The Presence of Asymmetric Transistor Aging **Variation-Aware Performance Verification of Analog Mixed-Signal Systems	P3.2 [Short] Fault-injection-Enhanced Virtual Prototypes Enable Early SW Development for Automotive Applications HW-SW-Coverification as part of CI/CD Integration Verification of Safety Components in Automotive Chip Modules [Short] Virtual ECUs with QEMU and SystemC TLM-2.0	P4.2 Accelerating Complex System Simulation using Parallel SystemC and FPGAs ** [Short] Design Verification of the Quantum Control Stack Control Flow Analysis for Bottom-up Portable Models Creation ** [Short] MetaPSS: An Automation Framework for Generation of Portable Stimulus Model	P5.2 Accelerate Functional Coverage Closure Using Machine-Learning-Based Test Selection A UVM Test-bench Skeleton Leveraging the Event Pool and Sequence Layering Towards a Hybrid Verification Environment for Signal Processing SoCs	

Technical Program Grid - Day 2 - November 15 (Cont)

	Forum 4	Forum 5	Forum 6	Forum 7	Forum 8	Großer Saal	
2:30 – 2:45 PM	Attendee Break (Großer Saal)						
2:45 – 3:45 PM	P1.3 The Three Body Problem Break the SoC with UVM Dynamically Generated Program Code	P2.3 Bridging the gap between system-level and chip-level performance optimization **MapGL: Interactive Application Mapping and Profiling on a Grid of Processing Cells	P3.3 Reverse Hypervisor - Faster SoC Simulation, an approach to Arm on Arm Efficient Debugging on Virtual Prototype using Reverse Engineering Method	P4.3 Verification Methodology for Efficient PVT(Process, Voltage and Temperature) Variation Analysis & Characterisation for Thermal and Power Aggressor IPs in a 3D SOC. Smart TSV (Thru Silicon Via) Repair Automation in 3DIC designs	P5.3 Plug and Play Verification: Leveraging Block-Level Components for Seamless Top-Level Integration The Road to Robustness: Addressing LPDDR5X PHY Verification Challenges with DFE		
3:45 – 4:00 PM	Attendee Break (Ballsaal)						Exhibit Hall Open
4:00 – 5:00 PM	P1.4 Planning for RISC-V Success: Verification Planning and Functional Coverage lead to quality RISC-V processor IP A Novel Approach to Standardise Verification Configurations using YAML	P2.4 **Evaluation of the RISC-V Floating Point Extensions **DSA Monitoring Framework for HW/SW Partitioning of Application Kernels leveraging VPs	P3.4 Grid-based Mapping and Analysis of a GoogLeNet CNN using MapGL Editor VPSim : Virtual Prototyping Simulator with best accuracy & execution time trade-off for High Performance Computing systems evaluation and benchmarking	P4.4 Testbench Linting – open-source way Effective Design Verification – Constrained Random with Python and Cocotb	P5.4 An Elegant scoreboard eco-system deploying UVM Callbacks, Parameterization for Multimedia designs from Imaging perspective Pragmatic Formal Verification Methodology for Clock Domain Crossing (CDC)		
5:00 – 6:00 PM	Panel: The Great Verification Chiplet Challenge (Ballsaal)						
6:00 – 6:30 PM	Closing Session & Best Paper Award (Ballsaal)						

** These are papers from the research track

Author presentations are 30-minutes in length unless listed as “[Short]” which will be a 15-minute presentation.

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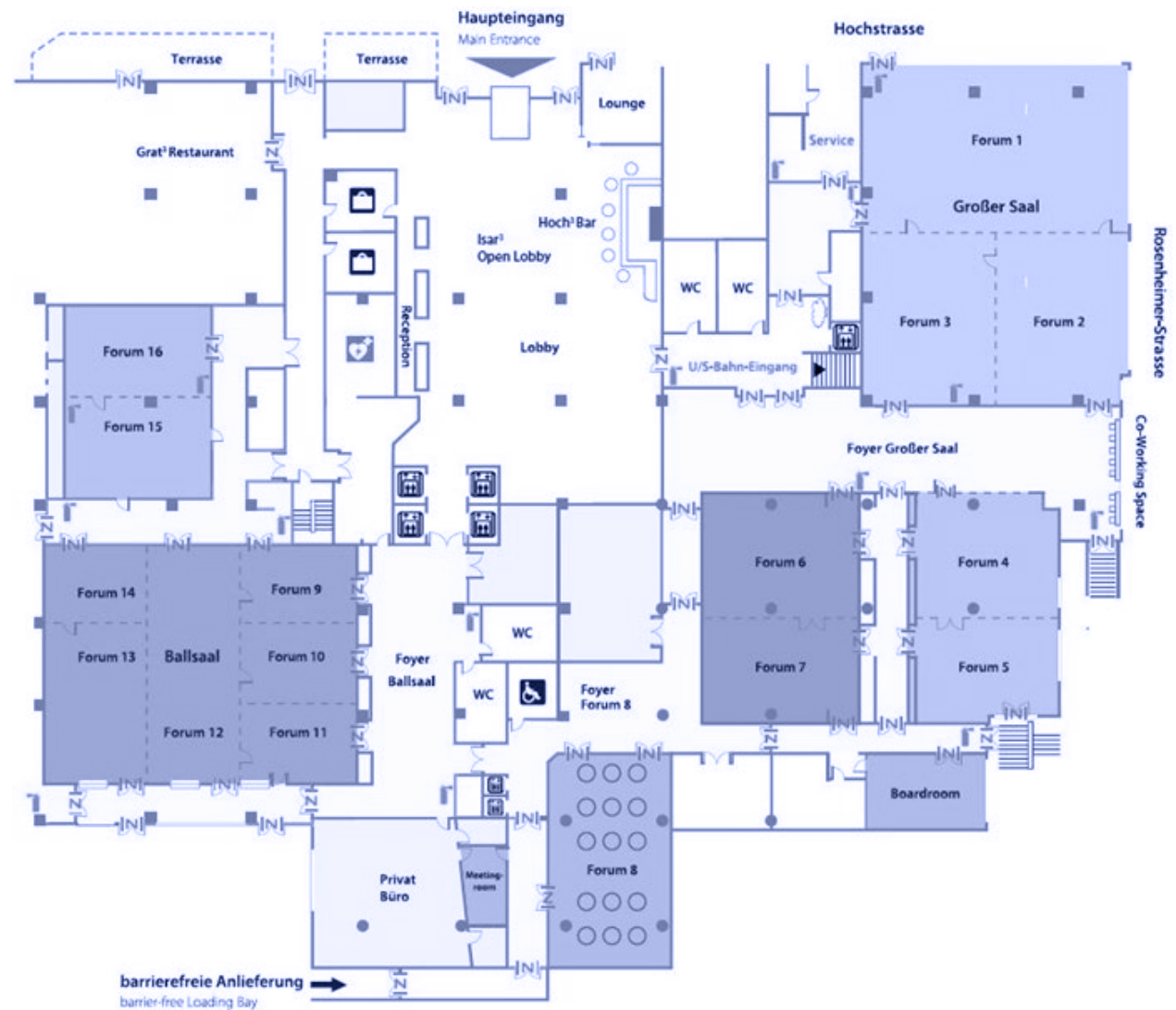
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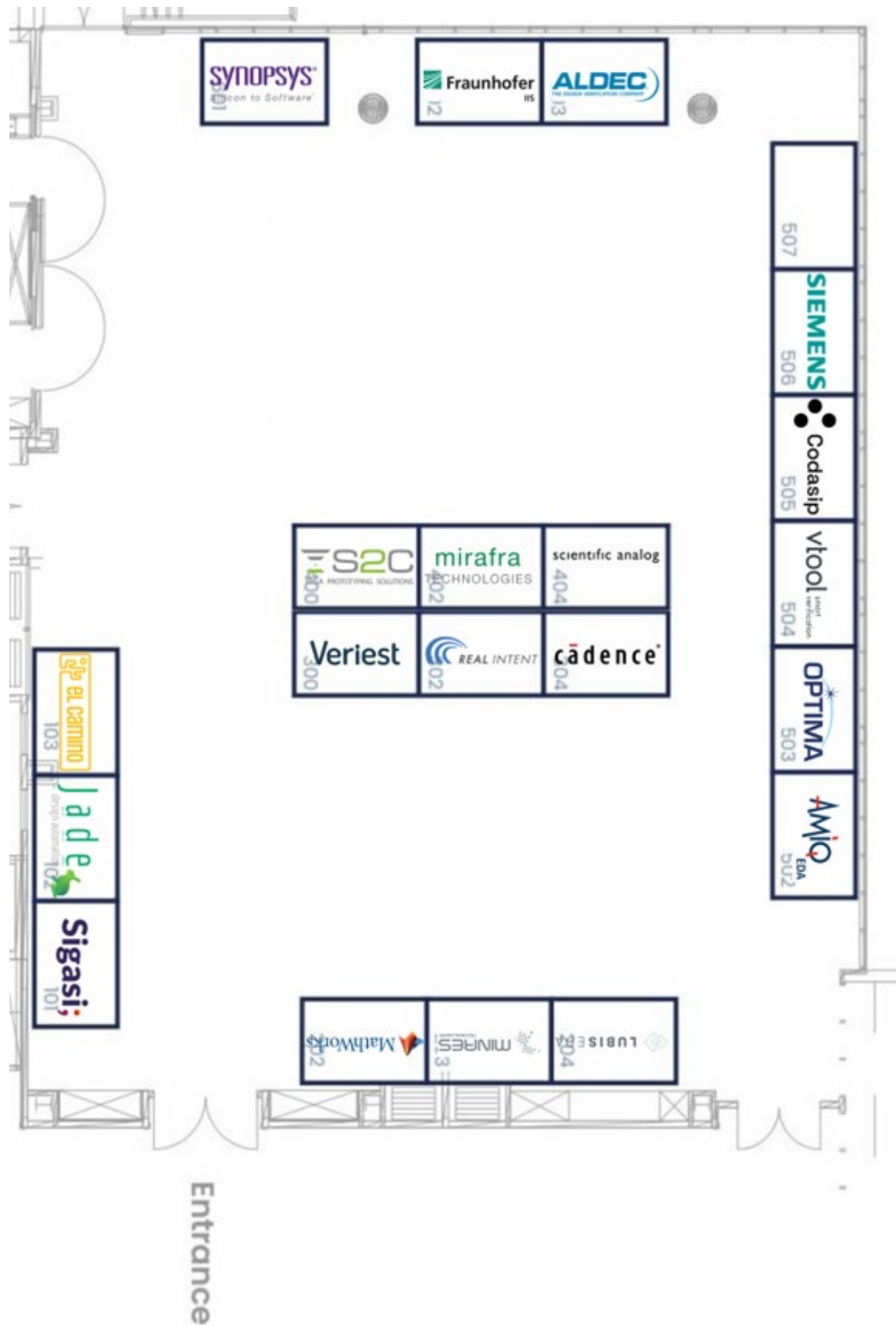
DVCon Europe 2023 Venue - Holiday Inn Munich City Centre

Hochstraße 3, 81669 München, Germany

The hotel is directly above Rosenheimer Platz S-Bahn station for fast, frequent connections across the city. It's a 10-minute train ride to Munich Hauptbahnhof and 35 minutes to Munich Airport (MUC). Families love the science and tech exhibits at the vast Deutsches Museum, a short walk away, while shoppers delight at the stores lining pedestrianised Kaufingerstrasse in the Old Town. The hotel has 18 meeting rooms offering space for up to 550 guests, and its convenient location makes it an ideal venue for events.



DVCon Europe 2023 Exhibit Hall – Großer Saal



Technical Program: Tuesday, November 14

Opening Session

8:30 AM – 8:45 AM

Ballsaal

Energy-efficient High Performance Compute, at the heart of Europe

8:45 AM – 9:45 AM



Ballsaal

Philippe Notton, SiPearl

Bio: Philippe Notton is the CEO and founder of SiPearl, the French company building the world's first energy-efficient HPC-dedicated microprocessor designed to work with any third-party accelerator (GPU, artificial intelligence, quantum).

As a senior executive, Philippe Notton has an outstanding track-record in the multimedia, semiconductor and security fields. Passionate about high technology and fast-moving environments, he has worked in France, the UK and the US for market-leading groups (Thomson, Canal+, LSI Logic, STMicroelectronics, Atos), as well as a successful startup (MStar Semiconductor, sold to MediaTek in 2012 for US\$4B).

Philippe Notton is a Supélec engineer (1993) and has an Executive MBA from ESSEC & Mannheim (2008).

Abstract: Today supercomputers are essential for meeting Europe major scientific industrial and societal challenges. But Europe is lagging behind in terms of supercomputing equipment. What's more, 100% of the microprocessor powering European supercomputers are non-European. This lack of sovereign technology has serious implications in highly strategic markets. To tackle this problem, Europe has launched EuroHPC JU and the European Processor Initiative (EPI). With a great success. In this talk, we will showcase how SiPearl -the private company born inside the EPI- is building the energy-efficient HPC dedicated microprocessor that will power Europe exascale supercomputers. We will particularly highlight SiPearl first generation microprocessor Rhea and how it will achieve its target to halve power consumption for the equivalent computing power. Thus, Rhea will contribute to meet strategic challenges for Europe while dramatically reducing the environmental footprint of supercomputing.

Attendee Break

9:45 AM – 10:00 AM

Großer Saal

Exhibit Hall Open

9:45 AM – 7:00 PM

Großer Saal

T1.1: IP-XACT Tutorial

10:00 AM – 11:30 AM

Forum 4

Edwin Dankert¹, Erwin de Kock², Devender Khari³, Jean-Michel Fernandez⁴, Michael Velten⁵, Thomas Steininger⁶

¹ARM Ltd., ²NXP Semiconductions, ³Agnisys, ⁴Arteris IP, ⁵Infineon, ⁶Intel

T2.1: Accellera Functional Safety Working Group Update and Next Steps

10:00 AM – 11:30 AM

Forum 5

Alessandra Nardi¹, Ghani Kanawati²,

¹Synopsys, ²ARM

Technical Program: Tuesday, November 14 (cont.)

T3.1: Scalable agile processor verification using SystemC UVM friends

10:00 AM – 11:30 AM

Forum 6

Presenters: Eyck Jentzsch, Stanislaw Kaushanski; Minres

T4.1: SysML v2: An overview with demonstration

10:00 AM – 11:30 AM

Forum 7

Prof. Dr. Christoph Grimm, University of Kaiserslautern

Attendee Break

11:30 AM – 11:45 AM

Großer Saal

T1.2: AI-Driven Debug and Verification Management

11:45 AM – 1:15 PM

Forum 4

Myles Glisson, Sr. Staff Applications Engineer; Synopsys Inc.

SYNOPSYS®

T2.2: Shift your HDL design left and keep your eyes on team code metrics in FPGA & ASIC design and verification

11:45 AM – 1:15 PM

Forum 5

Bart Brosens; Sigasi

Sigasi;

T3.2: Model-Based Approach for Developing Optimal HW/SW Architectures for AI systems

11:45 AM – 1:15 PM

Forum 6

Russell Klein, Petri Solanti; Siemens

SIEMENS

T4.2: New Methods in Core and SoC Verification based on RISC-V

11:45 AM – 1:15 PM

Forum 7

Adnan Hamid, David Kelf; Breker Verification Systems

 **BREKER™**

Lunch

1:15 PM – 2:15 PM

Großer Saal

T1.3: IP-XACT Industrial Practices

2:15 PM – 3:45 PM

Forum 4

Edwin Dankert¹, Erwin de Kock², Devender Khari³, Jean-Michel Fernandez⁴, Michael Velten⁵, Thomas Steininger⁶

¹ARM Ltd., ²NXP Semiconductions, ³Agnisys, ⁴Arteris IP, ⁵Infineon, ⁶Intel

Technical Program: Tuesday, November 14 (cont.)

T2.3: Migrating from UVM to UVM-MS

2:15 PM – 3:45 PM

Forum 5

Tim Pylant, Cadence

T3.3: Making the impossible possible: CDC and RDC closure with abstracts from different tools

2:15 PM – 3:45 PM

Forum 6

Jean-Christophe Brignone, STMicroelectronics

T4.3: Open-Source Virtual Platforms for Industry and Research

2:15 PM – 3:45 PM

Forum 7

Nils Bosbach, Rainer Leupers; Bosbach, Nils (RWTH Aachen University)

Attendee Break

3:45 PM – 4:00 PM

Großer Saal

T1.4: How to leverage the power of MATLAB from Functional Verification Test Benches

4:00 PM – 5:30 PM

Forum 4

Tom Richter; MathWorks



T2.4: The Expanding role of Static Signoff in Verification Coverage

4:00 PM – 5:30 PM

Forum 5

Oren Katzir, Vardan Vardanyan; Real Intent



T3.4: Exploring New Frontiers of High-Performance Verification with UVM-AMS

4:00 PM – 5:30 PM

Forum 6

Tim Pylant, Arumugan A; Cadence



T4.4: Double Software Verification Shift-left by combining Model-Based Design and Virtual ECUs'

4:00 PM – 5:30 PM

Forum 6

Dineshkumar Selvaraj¹, Tito Tang², Tim Kogel³,
¹Infiniteon Technologies, ²Mathworks, ³Synopsys



Reception

5:30 PM – 7:00 PM

Großer Saal

10th Anniversary Dinner

7:30 PM – 10:00 PM

Hofbräukeller

(Innere Wiener Straße 19, 81667 München, Germany)



Technical Program: Wednesday, November 15

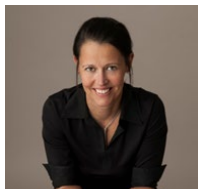
Opening Session

8:00 AM – 8:15 AM

Ballsaal

Keynote: Pervasive and Sustainable AI with Adaptive Computing

8:15 AM – 9:15 AM



Ballsaal

Michaela Blott, AMD Research

Bio: Michaela Blott is a Senior Fellow at AMD Research. She heads a team of international scientists driving exciting research in computer architectures for AI, green AI and agile compiler stacks. She earned a PhD from Trinity College Dublin and her Master's degree from the University of Kaiserslautern, Germany, and brings over 25 years of experience in leading-edge computer architecture and advanced FPGA and board design, in research institutions (ETH Zurich and Bell Labs) and development organizations. She is highly active in the research community as industrial advisor to numerous EU projects and research centres, serves on technical program committees, and received a number of Women in Tech Awards.

Abstract: In the context of AI, we face a plethora of challenges that extend beyond the widely discussed performance scalability required to meet the growing demands of compute and storage in the latest models. These challenges encompass sustainability, pervasiveness, agility, and diversity, all of which are needed to cater to a constantly evolving range of applications and algorithms from endpoint to edge and cloud. In this talk, we explore how AMD adaptive devices and agile compiler stacks can provide solutions by delivering post-production hardware specialization and co-designed algorithms. This results in highly optimized AI systems which not only provide the necessary performance scalability but also bring a reduction in carbon footprint while addressing the needs of a broad range of diverse applications with the necessary agility.

Panel: "All AI All the Time" Poses New Challenges for Traditional Verification

9:15 AM – 10:15 AM

Ballsaal

AI, including generative AI platforms such as ChatGPT, are straining data centers, hyperscalers and cloud computing, all the while optimizing and accelerating processes and creating new challenges for traditional verification technologies.

Verification tools have had some form of in-built intelligence for many years that would not be highlighted in any data sheet or whitepaper. Verification tool providers are now attempting to offer AI and machine learning capabilities within their functional verification solutions to improve performance and productivity, though questions remain on whether results are impressive enough to meet assumptions about current and future capabilities.

A panel that includes verification experts and vendors will attempt to determine how to best utilize AI/ML for functional verification and consider whether AI/ML-based verification tools will be able to keep up with the growing AI architecture design needs.

Attendees should be prepared for a discussion that addresses how the verification community will manage the emerging world of "All AI All the Time."

Audience participation will be encouraged.

Moderator:

- Paul Dempsey, Editor in Chief, Tech Design Forum

Panelists:

- Jean-Marie Brunet, Vice President and General Manager, Hardware-Assisted Verification, Siemens
- Micheala Blott, Senior Fellow, AMD
- Daniel Schostak, Arm Architect and Fellow, Verification, Arm
- Anil Deshpande, Director Engineering, Level 3 Certified Functional Safety Expert from TUV SUD, Samsung Semiconductor India Research
- Lu Dai, Senior Director of Engineering, Qualcomm

Technical Program: Wednesday, November 15 (cont.)

Attendee Break

10:15 AM – 10:30 AM

Großer Saal

Exhibit Hall Open

10:15 AM – 6:00 PM

Großer Saal

P1.1

10:30 AM – 12:00 PM

Forum 4

A Hybrid Approach For Interrupts Verification

Dr. Giovanni Auditore MdB¹; Dr. Qibo Peng MdB²; Dr. Francesco Rua' MdB¹

¹ STMicroelectronics srl; ² Politecnico di Torino

Verification of an AXI cache controller using multi-thread approach based on OOP design patterns

Dr. Francesco Rua' MdB¹; Péter Sági²

¹ STMicroelectronics srl; ² Veriest Solutions

[Short] Hybrid Emulation for faster Android Home screen bring up and Software Development

Sarang Kalbande¹; Manoj Khandelwal¹; Sarang Kalbande¹; Garima Srivastava¹;

Hyundon Kim²

¹ Samsung Semiconductor India R & D Centre(SSIR); ² Samsung Electronics, Korea

[Short] A perfect blend of verification techniques, platforms, and AI-empowered debugging in Ethernet Subsystem Verification

Tijana Misic; Olivera Stojanovic

Vtool doo

P2.1

10:30 AM – 12:00 PM

Forum 5

A SV VQC UDN for Modeling Switch-Capacitor-based Circuits

PhD Yi Wang

Renesas Electronics Cooperation

Self-Triggering Mechanism for Modeling a Low-Dropout Regulator with Load Capacitor

Mariska van der Struijk; Yi Wang

Renesas Electronics Cooperation

****[Short] On the Performance Differences of SystemC and SystemC AMS: A Guideline for Real Number Modeling and Beyond**

Alexandra Küster¹; Dr. Rainer Dorsch¹; Prof. Dr. Christian Haubelt ssdd²

¹ Bosch Sensortec GmbH; ² University of Rostock

****[Short] A tool for Investigating Cyber-Physical Systems via SystemC AMS Virtual Prototypes Derived from SysML Models**

Dr. Daniela Genius¹; Prof. Ludovic Apvrille²

¹ Sorbonne Université – LIP6; ² Télécom Paris, Institut Polytechnique de Paris

Technical Program: Wednesday, November 15 (cont.)

P3.1

10:30 AM – 12:00 PM

Forum 6

[Short] A Model-Based Reusable Framework to Parallelize Hardware and Software Development

Tom Richter¹; Jouni Sillanpää²; Hakan Pettersson¹

¹ MathWorks; ² Nokia

Fuzzing Firmware running on Intel® Simics® Virtual Platforms

PhD Jakob Engblom; Dr. Robert Guenzel

Intel Corporation

[Short] 400G IPU Case Study: Demonstrating Shift-left of Soft Logic RTL Development on Real World Design using Intel Agilex FPGA SystemC Model

Pravat Kishor Nayak¹; Vikrant Kapila²; Pushpa Naik¹; Niketkumar Natvarbhai Sharma¹

¹ Intel Technology India Pvt Ltd; ² Intel Technology Asia Pte Ltd

****Co-Design of Automotive Boardnet Topology and Architecture**

Sebastian Post; Prof. Dr. Christoph Grimm

P4.1

10:30 AM – 12:00 PM

Forum 7

Verilator + UVM-SystemC: a match made in heaven

Luca Sasselli; Qualcomm

Closed-Loop Model-First SoC Development With the Intel Simics Simulator

Kalen Brunham; Anthony Moore; Tobias Rozario; Wei Jun Yeap; PhD Jakob Engblom
Intel Corporation

**** [Short] A Compositional Simulation Framework for Testing Adversarial Robustness of Deep Neural Networks**

Youssef Maher Nader¹; Mostafa Lotfy Hatab¹; Mazen Mostafa Ghaleb¹; Safia Medhat Bakr¹; Tasneem A. Awaad¹; Ahmed AlGanzouri²; Dr. Mohamed Abdelsalam²;

Prof. Dr. M. Watheq El-Kharashi¹

¹ Faculty of Engineering, Ain Shams University; ² Siemens EDA

**** [Short] Large-scale Gatelevel Optimization Leveraging Property Checking**

Lucas Klemmer MSc.; Dominik Bonora; Univ.-Prof. Dr Daniel Große

Johannes Kepler University Linz

Technical Program: Wednesday, November 15 (cont.)

P5.1

10:30 AM – 12:00 PM

Forum 8

[Short] An Improved Methodology for Debugging UPF Issues at SoC level Power Aware Simulations

Ruchi Misra; Shrinidhi Rao; Alok Kumar; Garima Srivastava
Samsung Semiconductor India R & D Centre(SSIR)

Unified Architecture of L1 and L2 Cache with Low Power Extensions for Multi-Core UVM-based Library Package

Avnita Pal; Priyanka Gharat; Sastry Puranapanda; Darshan Sarode
Silicon Interfaces

Virtual testing of overtemperature protection algorithms in automotive smart fuses

Thomas Markwirth¹; Gabriel Pachiana¹; Dr. Christoph Sohrmann¹; Mehdi Meddeb²; Gunnar Bublitz²; Heinz Wagensohn²

¹ Fraunhofer IIS/EAS; ² CARIAD SE (Volkswagen Group)

[Short] Efficient Verification of a RADAR SoC Using Formal and Simulation-Based Methods

Aman Kumar¹; Mark Litterick²; Samuele Candido¹

¹ Infineon Technologies Dresden GmbH & Co. KG; ² Verilab GmbH

Lunch

12:00 PM – 1:00 PM

Großer Saal

P1.2

1:00 PM – 2:30 PM

Forum 4

A scalable VIP component to increase robustness of co-verification within an ASIC

Mario de Matteis; Matteo Barbati
ON Semiconductor

A Novel Framework to Accelerate System Validation on Emulation

Sarang Madhukarrao Kalbande¹; Rinkesh Yadav¹; Sarang Kalbande¹; Garima Srivastava¹; Hyundon Kim²

¹ Samsung Semiconductor India R & D Centre(SSIR); ² Samsung Electronics, Korea

[Short] Low-Power Validation Framework for Standard Cell Library including Front-End and Back-End implementation

Jinho Lee¹; Hyunju Bak¹; SangGi Do¹; Taejun Yoo¹; Gowrishankar Srinivasan²; Vishw Mitra Singh Bhadouria²

¹ Samsung Electronics; ² Samsung Semiconductor India R & D Centre(SSIR)

[Short] Initialization Techniques for D-Flip-Flop Based Scan Chain with Scan Flush Architecture in Gate-Level Simulation

Wei Jun Yeap; Rahul Chauhan
Intel

Technical Program: Wednesday, November 15 (cont.)

P2.2

1:00 PM – 2:30 PM

Forum 5

System-Level Simulation of a SPAD-Based Time-of-Flight Sensor in SystemVerilog

Seungah Park¹; Dr. Hyeongseok Seo²; Dr. Canxing Piao²; Jaemin Park³; Prof. Jaehyuk Choi⁴; Prof. Jung-Hoon Chun⁴

¹ Sungkyunkwan University (SKKU); ² SolidVue Inc.; ³ Scientific Analog Inc.; ⁴ Sungkyunkwan University (SKKU), SolidVue Inc.

****Clock Tree Design Considerations in The Presence of Asymmetric Transistor Aging**

Prof. Dr. Freddy Gabbay PhD¹; Firas Ramadan²; Majd Ganaiem²

¹ Ruppin Academic Center, Israel; ² Technion – Israel Institute of Technology

****Variation-Aware Performance Verification of Analog Mixed-Signal Systems**

Dr.-Ing. Carna Zivkovic¹; Jan Rödel²; Neha Chavan²; Prof. Dr. Christoph Grimm³; Frank Rethmeier²

¹ NXP Semiconductors; ² NXP Semiconductors Germany GmbH; ³ RPTU Rheinland-Pfälzische Technische Universität

P3.2

1:00 PM – 2:30 PM

Forum 6

[Short] Fault-injection-Enhanced Virtual Prototypes Enable Early SW Development for Automotive Applications

Dr. Mohammad Badawi PhD; Javier Castillo; Dr. Andreas Mauderer PhD; Dr. Jan-Hendrik Oetjens

Robert Bosch GmbH

HW-SW-Coverification as part of CI/CD

Johannes Grinschgl¹; Ganesh Rajasekharan Nair²; Alexander Hoffmann³; Nan Ni

¹ Infineon Technologies AG, Neubiberg, Germany; ² Infineon Technologies AG Neubiberg, Germany; ³ Infineon Technologies AG

Integration Verification of Safety Components in Automotive Chip Modules

Dr. Holger Busch

Infineon Technologies

[Short] Virtual ECUs with QEMU and SystemC TLM-2.0

Lukas Jünger¹; Dr. Jan Henrik Weinstock¹; Munish Jassi²; Hitoshi Hamao³; Megumi Yoshinaga³; Koichi Sato³

¹ MachineWare GmbH; ² Renesas Electronics Europe GmbH;

³ Renesas Electronics Corporation

Technical Program: Wednesday, November 15 (cont.)

P4.2

1:00 PM – 2:30 PM

Forum 7

Accelerating Complex System Simulation using Parallel SystemC and FPGAs

Stanislaw Kaushanski¹; Johannes Wirth²; Eyck Jentzsch¹; Andreas Koch²

¹ MINRES Technologies GmbH; ² Technische Universität Darmstadt

** [Short] Design Verification of the Quantum Control Stack

Samin Ishtiaq; Rojalin Mishra; Dr. Seyed Amir Alavi PhD; Dr. Nick Johnson; Dwaraka O N; Asher Pearl

Riverlane

Control Flow Analysis for Bottom-up Portable Models Creation

Petr Bardonek; Marcela Zachariášová PhD

Brno University of Technology, Faculty of Information Technology

** [Short] MetaPSS: An Automation Framework for Generation of Portable Stimulus Model

Jaimini Nagar¹; Thorsten Dworak²; Sebastian Simon¹; Ulrich Heinkel³; Djones Lettnin²

¹ Infineon Technologies Dresden GmbH & Co. KG; ² Infineon Technologies AG Munich; ³ Technical University Chemnitz

P5.2

1:00 PM – 2:30 PM

Forum 8

Accelerate Functional Coverage Closure Using Machine-Learning-Based Test Selection

Jakub Pluciński¹; Łukasz Bielecki¹; Robert Synoczek¹; Emelie Andersson²; Antti Löytynoja²; Cristian Macario²

¹ Nokia; ² MathWorks

A UVM Test-bench Skeleton Leveraging the Event Pool and Sequence Layering

Marcela Zachariasova PhD¹; Tomáš Pehnelt; Jiri Bartak; Jan Riha

¹ ASICentrum, EM Microelectronic

Towards a Hybrid Verification Environment for Signal Processing SoCs

Jan Hahlbeck; Steffen Löbel; Chandana G.P.

NXP Semiconductors Germany GmbH

Attendee Break

2:30 PM – 2:45 PM

Großer Saal

P1.3

2:45 PM – 3:45 PM

Forum 4

The Three Body Problem

Peter Birch¹; Ben Marshall²

¹ VyperCore; ² PQShield

Break the SoC with UVM Dynamically Generated Program Code

Bogdan Todea; Madhukar Mahadevappa

Microchip Technology

Technical Program: Wednesday, November 15 (cont.)

P2.3

2:45 PM – 3:45 PM

Forum 5

Bridging the gap between system-level and chip-level performance optimization

Soniya Gupta¹; Vikrant Kapila²; Holger Keding³; Tim Kogel³

¹ Synopsys India Pvt. Ltd.; ² Intel Inc (Singapore); ³ Synopsys Inc Aachen Germany

****MapGL: Interactive Application Mapping and Profiling on a Grid of Processing Cells**

Dr. Claudio Raccomandato¹; Prof. Emad Malekzadeh Arasteh²; Prof. Rainer Dömer²

¹ Politecnico di Torino; ² University of California, Irvine

P3.3

2:45 PM – 3:45 PM

Forum 6

Reverse Hypervisor – Faster SoC Simulation, an approach to Arm on Arm on Arm

François-Frédéric Ozog¹; Mark Burton²

¹ Shokubai.tech; ² QUALCOMM

Efficient Debugging on Virtual Prototype using Reverse Engineering Method

Sandeep Puttappa; Dineshkumar Selvaraj; Ankit Kumar

Infineon Technologies

P4.3

2:45 PM – 3:45 PM

Forum 7

Verification Methodology for Efficient PVT (Process, Voltage and Temperature) Variation Analysis & Characterisation for Thermal and Power Aggressor IPs in a 3D SOC.

Jasobanta Sahoo Jaso; Vineeth Rao Vineeth; Sekhar DANGUDUBIYYAM

Samsung Semiconductor India R & D Centre(SSIR)

Smart TSV (Thru Silicon Via) Repair Automation in 3DIC designs

Subramanian R; Jyoti Verma; Naveen Srivastava; Sekhar Dangudubiyam

Samsung Semiconductor India R & D Centre(SSIR)

P5.3

2:45 PM – 3:45 PM

Forum 8

Plug and Play Verification: Leveraging Block-Level Components for Seamless Top-Level Integration

Tchiya Dayan

Mobileye

The Road to Robustness: Addressing LPDDR5X PHY Verification Challenges with DFE

Chethan Gowdra Bomanna; Muhammed Asif Kavil Thodukayil; Anil Deshpande

Samsung Semiconductor India R & D Centre(SSIR)

Attendee Break

3:45 PM – 4:00 PM

Großer Saal

Technical Program: Wednesday, November 15 (cont.)

P1.4

4:00 – 5:00 PM

Forum 4

Planning for RISC-V Success: Verification Planning and Functional Coverage lead to quality RISC-V processor IP

Aimee Sutton¹; Duncan Graham¹; Simon Davidmann¹; Pascal Gouedo²; Yoann Pruvost²; Xavier Aubert²

¹ Imperas Software Ltd.; ² Dolphin Design

A Novel Approach to Standardise Verification Configurations using YAML

Nikhil Tambekar

Nokia Solutions and Networks Oy

P2.4

4:00 – 5:00 PM

****Evaluation of the RISC-V Floating Point Extensions**

Niko Zurstraßen¹; Lennart Michael Reimann¹; Nils Bosbach¹; Lukas Jünger²; Rainer Leupers¹

¹ RWTH Aachen University; ² MachineWare GmbH

****DSA Monitoring Framework for HW/SW Partitioning of Application Kernels leveraging VPs**

Christoph Hazott MSc.; Prof. Dr. Daniel Große

Johannes Kepler Universität Linz

P3.4

4:00 – 5:00 PM

Forum 6

Grid-based Mapping and Analysis of a GoogLeNet CNN using MapGL Editor

Dr. Claudio Raccomandato¹; Prof. Emad Arasteh²; Prof. Rainer Dömer²

¹ Politecnico di Torino; ² University of California, Irvine

VPSim : Virtual Prototyping Simulator with best accuracy & execution time trade-off for High Performance Computing systems evaluation and benchmarking

Ayoub Mouhagir; Mohamed Benazouz PhD; Lilia Zaourar PhD

CEA

P4.4

4:00 – 5:00 PM

Forum 7

Testbench Linting – open-source way

Srinivasan Venkataramanan¹; Deepa Palaniappan¹; Satinder Paul Singh²

¹ AsFigo Technologies; ² Cogknit EU

Effective Design Verification – Constrained Random with Python and Cocotb

Suruchi Kumari¹; Deepak Narayan Gadde

¹ Infineon

Technical Program: Wednesday, November 15 (cont.)

P5.4

4:00 – 5:00 PM

Forum 8

An Elegant scoreboard eco-system deploying UVM Callbacks,Parameterization for Multimedia designs from Imaging perspective

Chakravarthi Devakinanda Vurukutla¹; Sahana Ranganathan; Devendra Satish Bilaye; Vivek Kumar; Karthik Majeti

¹ Samsung Semiconductor India Research

Pragmatic Formal Verification Methodology for Clock Domain Crossing (CDC)

Aman Kumar¹; Muhammad Ul Haque Khan²; Bijitendra Mittra²

¹ Infineon Technologies Dresden GmbH & Co. KG; ² Cadence Design Systems

Panel: The Great Verification Chiplet Challenge

5:00 – 6:00 PM

Ballsaal

Chiplet technology represents a paradigm shift in semiconductor design, heralding a new era of more modular and efficient approach to building complex systems-on-chip (SoCs). The latest trend racing through the semiconductor industry is the move to chiplets as companies are invigorating themselves to stay on the cutting edge of technology. Or so it seems as European and U.S. companies embrace a chiplet strategy to overcome Moore's Law and continue boosting the performance of their latest devices. Overlooked in the heady rush to chiplets are necessary changes to verification to meet the interfacing requirements of a complex chiplet structure.

DVCon Europe presents "The Great Verification Chiplet Challenge" panel featuring Moderator Nick Flaherty who will referee a free-form discussion to unravel the thorny questions about advancing verification to support chiplets and the emerging UCle interconnect chiplets standard. Panelists from a cross-section of the chip and design verification community will address the chiplet factor facing verification methodologies and why verification must expand beyond functional block tests. The panel will explore strategies for comprehensive verification, including the role of simulation, emulation, and hardware/software co-verification in ensuring the reliability and functionality of chiplet-based systems.

Panelists will conclude by casting a discerning eye toward areas for improvement throughout the verification flow for all chip design. Attendees can expect spirited and lively insights and plenty of good humor.

Audience participation will be encouraged and welcome during what is destined to be an interesting and informative hour-long session.

Moderator:

- Nick Flaherty, Editor-in-Chief, eeNews Europe

Panelists:

- Axel Jahnke, MN SoC R&D Manager, Nokia
 - Bodo Hoppe, Distinguished Engineer Hardware Verification, IBM
 - Ashish Darbari, CEO and Founder, Axiomise
 - David Kelf, CEO, Breker Verification Systems
 - Moshe Zalcborg, CEO, Veriest
-

Closing Session & Best Paper Award

6:00 – 6:30 PM

Ballsaal

SystemC Evolution Day 2023

Workshop on the Evolution of SystemC Standards: 16 November 2023

The eight SystemC Evolution Day is a full-day, technical workshop on the evolution of SystemC standards to advance the SystemC ecosystem. In several in-depth sessions, selected current and future standardization topics around SystemC will be discussed in order to accelerate their progress for inclusion in Accellera/IEEE standards.

SystemC Evolution Day is intended as a lean, user-centric, hands-on forum bringing together experts from the SystemC user community and the Accellera Working Groups to advance SystemC standards.

Theme this year

The main theme this year is The future of SystemC: With the release of the updated SystemC standard IEEE 1666-2023 in September, the community will reflect on the future of SystemC and discuss the possible and essential steps in the SystemC standardization journey.

Agenda

Note: This is a face-to-face event, so no online presentations / participation possible

Time (CET)	Title	Presenter(s), Organization
09:30 - 10:00	Welcome & Introduction – Theme: Evolution and Ecosystem	Mark Burton, SystemC Evolution Day Chair
10:00 - 11:00	SystemC Language Working Group and IEEE 1666-2023 Update	Laurent Mailliet-Contoz, SystemC LWG Chair
11:00 - 11:30	Accellera SystemC Working Groups update	Martin Barnasconi, Accellera Technical Committee Chair
11:30 - 12:00	New Federated Simulation Standard Proposed Working Group	Mark Burton, FSS PWG Vice-chair
12:00 - 12:30	Trace features in SystemC	Lukas Jünger, MachineWare GmbH Eyck Jentzsch, MINRES Technologies
12:30 - 14:00	Lunch	
14:00 - 14:30	RISC-V VP++: Unlocking the vast Linux ecosystem for Open Source RISC-V Virtual Prototypes: From Fast Bootup, VNC, Vector Extension to 3D-Games	Daniel Große, JKU Linz, Austria
14:30 - 15:30	The Future of SystemC	Discussion - All
15:30 - 17:00	SystemC Configuration Control Inspection : Where do we go from here !	Lukas Jünger, CCI WG Chair
17:00 - 17:15	Wrap-up & closure	



Save the Date!

DVCon Europe 2024

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October 15-16, 2024